10.7 DIGITAL LOGIC CURRENT FLOW

As discussed in the previous section, the lowest impedance (inductance) signal return path for high-frequency current is in a plane directly adjacent the signal trace. In the case of the four-layer printed circuit board stackup shown in Fig. 10-30, the return current path for the signal on the top layer will be the power plane. As discussed previously, the electric field lines that result from the signal on a microstrip trace terminate on the adjacent plane, as was shown in Fig. 10-7, regardless of what the purpose of the plane is. Because at high frequencies the fields cannot penetrate the plane, due to skin effect, the signal does not know that there is a ground plane below the power plane, and therefore the return current will be on the power plane. Does this create a problem? Is it not better to have the return current on the ground plane? To answer these questions, we must first analyze how the digital logic signal currents actually flow.

Many engineers and designers are confused about how and where digital return currents flow and what is the source of the digital logic current. First, let me state that *the driver IC is not the source of the current*; the IC only acts as a switch, to direct the current. The source of the current is the decoupling capacitor and/or the parasitic trace and load capacitance.

Only the transient (switching) current is important from a noise or EMC perspective, and the transient current flow does not depend on the load at the end of the line (see discussion associated with Fig. 5-19). Because the propagation time of the line is finite, the transient current does not know what the load impedance is until after the signal has already transversed the line.

The return current path is a function of the topology of the transmission line, stripline or microstrip, and on whether the logic transition is a high-to-low or a low-to-high transition. Also, in the case of a microstrip line, the return current path is a function of whether the trace is adjacent to a ground or power plane, and in the case of a stripline whether the trace is located between two ground planes, two power planes, or one ground and one power plane.

Figure 10-31 shows the circuit of a CMOS logic gate with its output signal trace located between a power and ground plane, which is a stripline configuration. Also shown in the figure are the load IC, the source's decoupling capacitor, the parasitic capacitance of the signal trace, and the load capacitance. Figures 10-32 to 10-37 show the logic current paths for the various possible configurations.

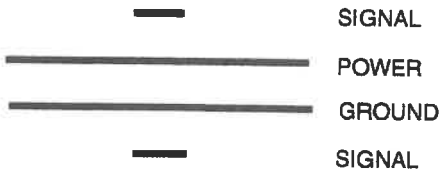

FIGURE 10-30. A common four-layer printed circuit board stackup.

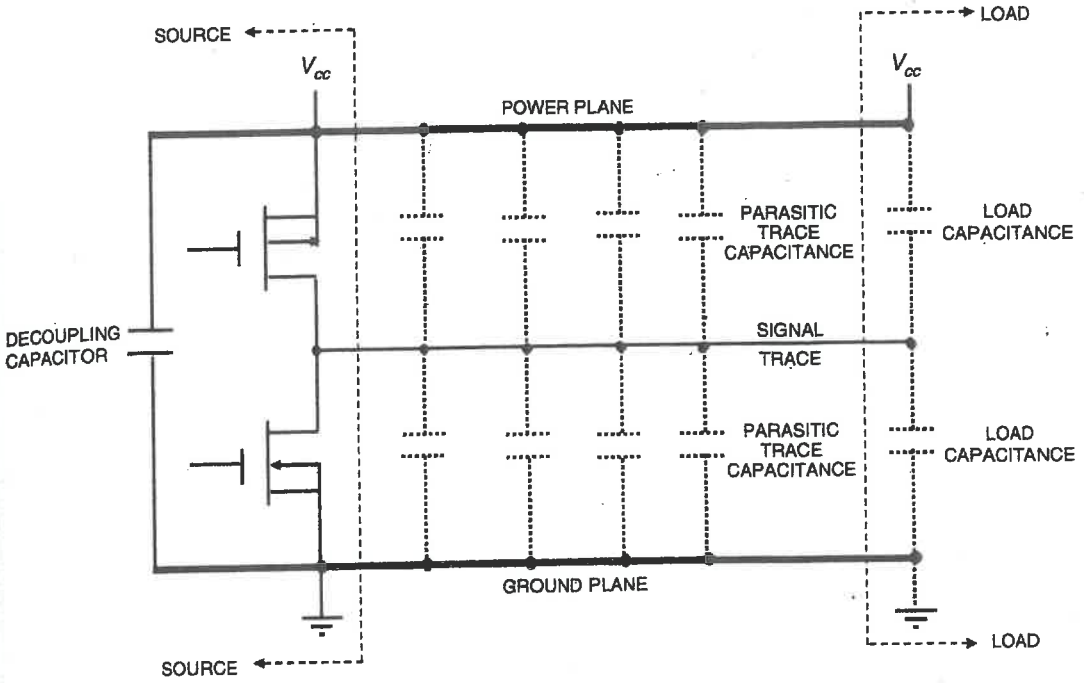

FIGURE 10-31. Circuit of a CMOS logic gate driving a stripline located between a power and ground plane.

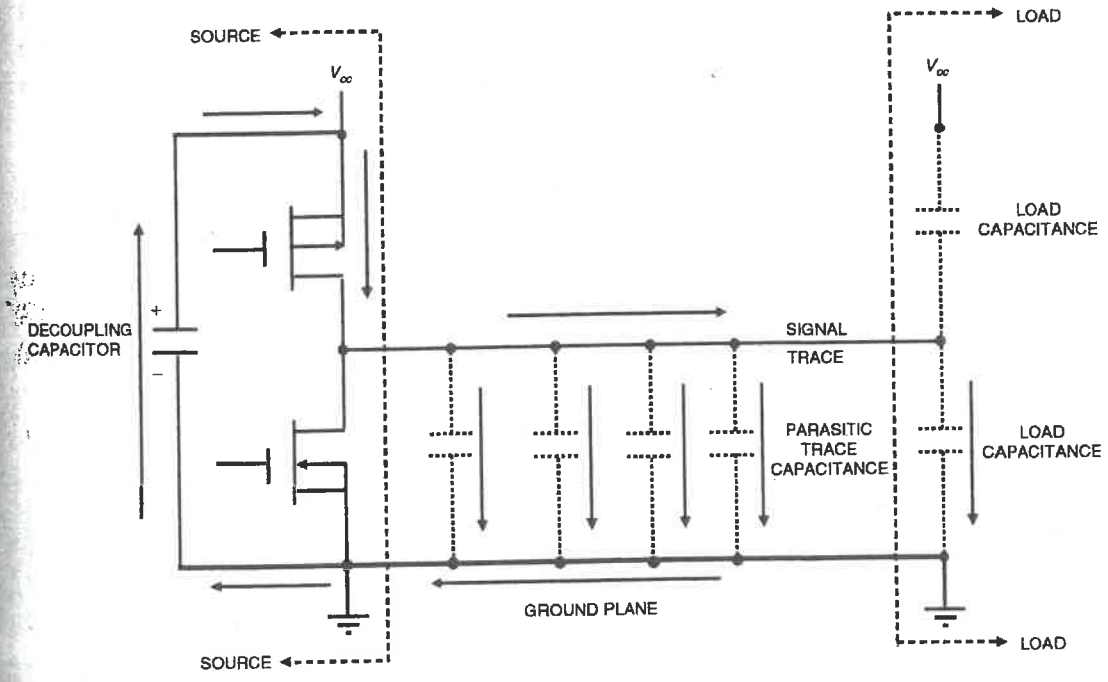

FIGURE 10-32. Current flow on a microstrip line adjacent to a ground plane, low-to-high transition.

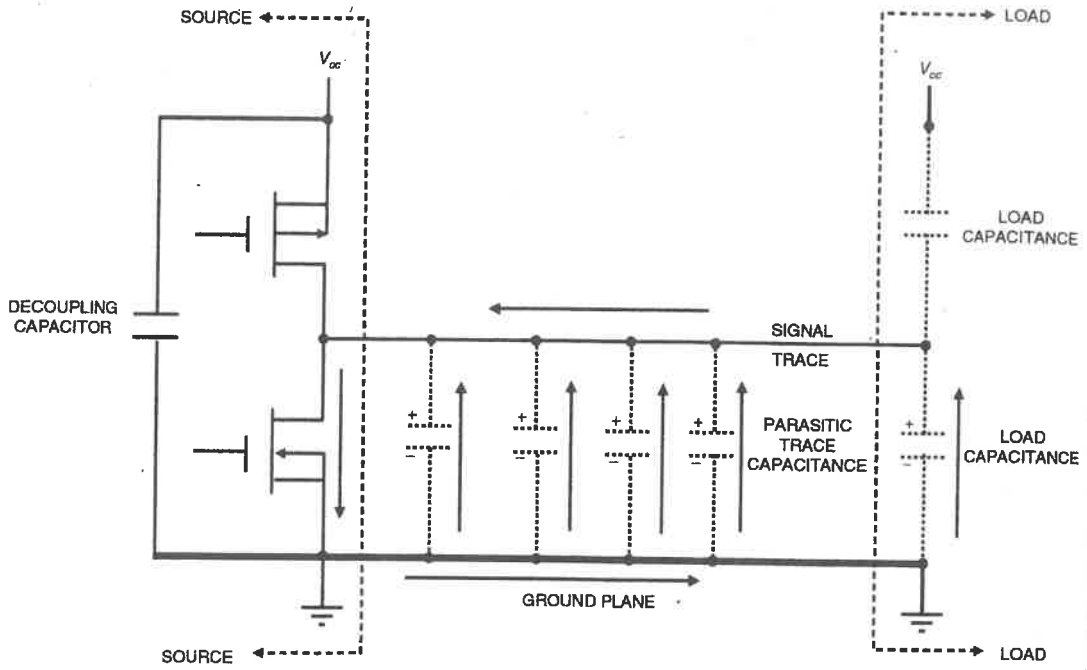

FIGURE 10-33. Current flow on a microstrip line adjacent to a ground plane, high-to-low transition.

10.7.1 Microstrip Line

Figure 10-32 shows the current path for a low-to-high transition on a microstrip line adjacent to a ground plane. As can be observed, the current source is the decoupling capacitor. The current flows through the upper transistor of the CMOS logic gate, down the signal trace toward the load, through the trace to ground parasitic capacitance,* and returns to the decoupling capacitor on the ground plane.

Figure 10-33 shows the current path for a high-to-low transition on a microstrip line adjacent to a ground plane. As can be observed, the current source is the trace-to-ground parasitic capacitance. The current flows down the signal trace toward the driver IC, through the lower transistor of the CMOS driver, and returns on the ground plane. In this case, it is the lower transistor of the CMOS driver shorting out the trace-to-ground capacitance that produces the current flow. Note that in this case, the decoupling capacitor is not involved in the current path.

Figure 10-34 shows the current path for a low-to-high transition on a microstrip line adjacent to a power plane. As can be observed, the current source is the trace-to-power plane parasitic capacitance. The current flows down the power plane toward the source, through the upper transistor of the

* In this section, whenever I refer to the parasitic trace-to-ground capacitance, I mean the parasitic trace capacitance plus the load capacitance.

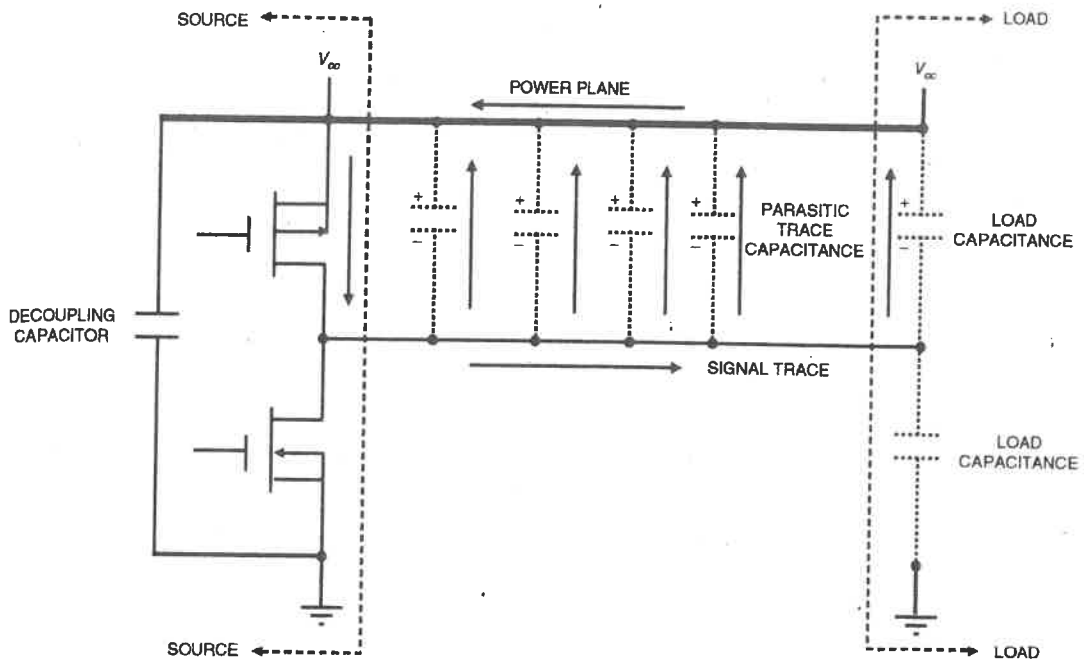

FIGURE 10-34. Current flow on a microstrip line adjacent to a power plane, low-to-high transition.

CMOS driver, and returns on the signal trace. In this case, it is the upper transistor of the CMOS driver shorting out the trace-to-power plane capacitance that produces the current flow. As in the previous case, the decoupling capacitor is not involved in the current path.

Figure 10-35 shows the current path for a high-to-low transition on a microstrip line adjacent to a power plane. As can be observed, the current source is the decoupling capacitor. The current flows through the power plane, through the trace-to-power plane capacitance, returns to the driver IC on the signal trace, and flows through the lower transistor of the driver back to the decoupling capacitor.

10.7.2 Stripline

Figure 10-36 shows the current path for a low-to-high transition on a stripline located adjacent to both a power and a ground plane. As can be observed, the current source is the decoupling capacitor *plus* the trace-to-power plane parasitic capacitance. The decoupling capacitor current (solid arrow) flows through the top transistor of the CMOS driver, down the signal trace toward the load, through the parasitic trace-to-ground plane capacitance, and returns to the decoupling capacitor on the ground plane. The trace-to-power plane capacitance current (dashed arrow) flows on the power plane back toward the driver IC, through the top driver transistor, and returns on the signal trace. Notice that for this configuration, current flows on both the

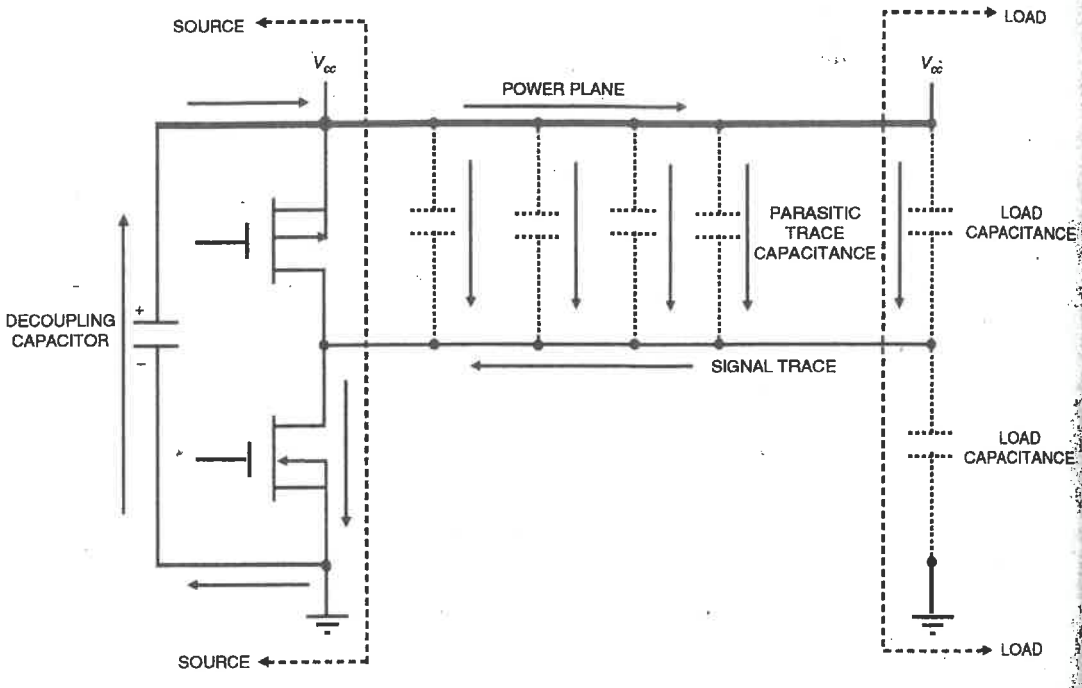

FIGURE 10-35. Current flow on a microstrip line adjacent to a power plane, high-to-low transition.

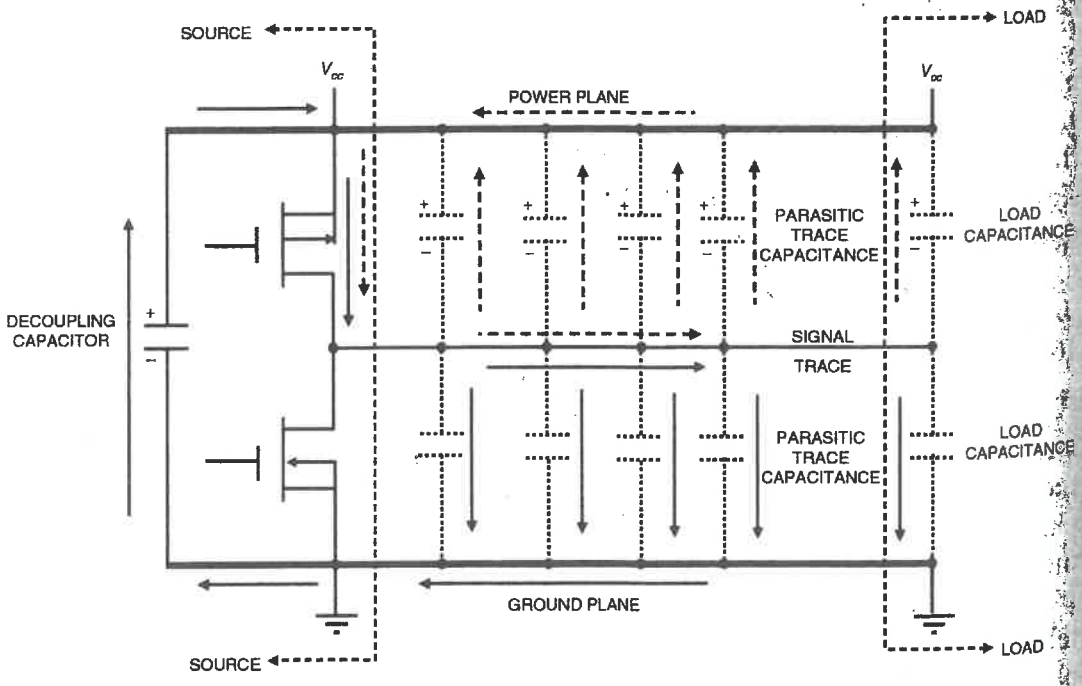

FIGURE 10-36. Current flow on a stripline adjacent to both a ground and a power plane, low-to-high transition.

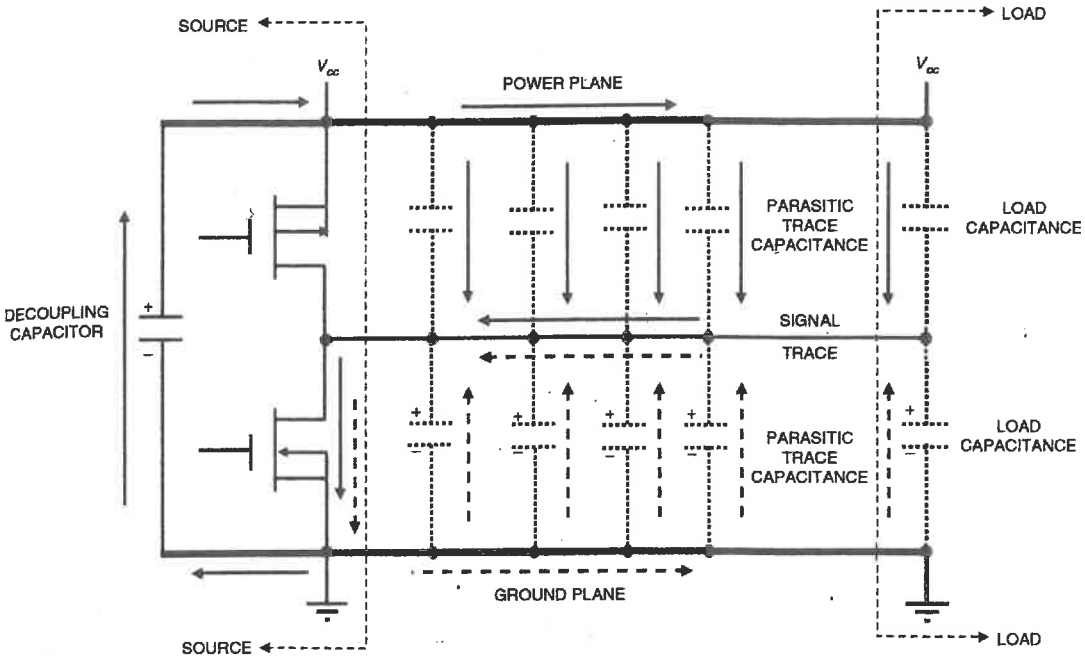

FIGURE 10-37. Current flow on a stripline adjacent to both a ground and a power plane, high-to-low transition.

ground and the power planes, and that the current in both planes flows in the same direction, in this case, from the load toward the source.

Figure 10-37 shows the current path for a high-to-low transition on a stripline located adjacent to both a power and ground plane. As can be observed, the current source is the decoupling capacitor *plus* the trace-to-ground plane capacitance. The decoupling capacitor current (solid arrow) flows down the power plane, through the trace-to-power plane capacitance, back to the driver IC on the signal trace, and through the bottom transistor of the CMOS driver back to the decoupling capacitor. The trace-to-ground plane capacitance current (dashed arrow) flows on the signal trace back toward the driver IC, through the bottom driver transistor, and returns on the ground plane. Notice that for this configuration, current also flows in the same direction on both the ground and the power planes; but in this case, the current direction is from the source toward the load.

For the case of a stripline referenced to two ground planes, the current source and current path are the same as the case of a microstrip line referenced to a ground plane (Figs. 10-32 and 10-33), except that in the stripline case, each plane carries only one half the total current. For the case of a stripline referenced to two power planes, the current flow is the same as the case of a microstrip line referenced to a power plane (Figs. 10-34 and 10-35), except in the stripline case, each plane carries only one half the total current.

In all the stripline cases, the current flows in two different signal loops, and the current in the two loops flows in the opposite direction, counter clockwise (CCW) in one loop and clockwise (CW) in the other loop, and in addition each